PRODUCT SPECIFICATION

AMOLED MODULES

Model No：ZXYQ667009

For Customer's Acceptance	
Approved by	**Comment**

	Signature	Date
Prepared by	**WJH**	**2023.8.26**
Checked by	**WJH**	**2023.8.26**
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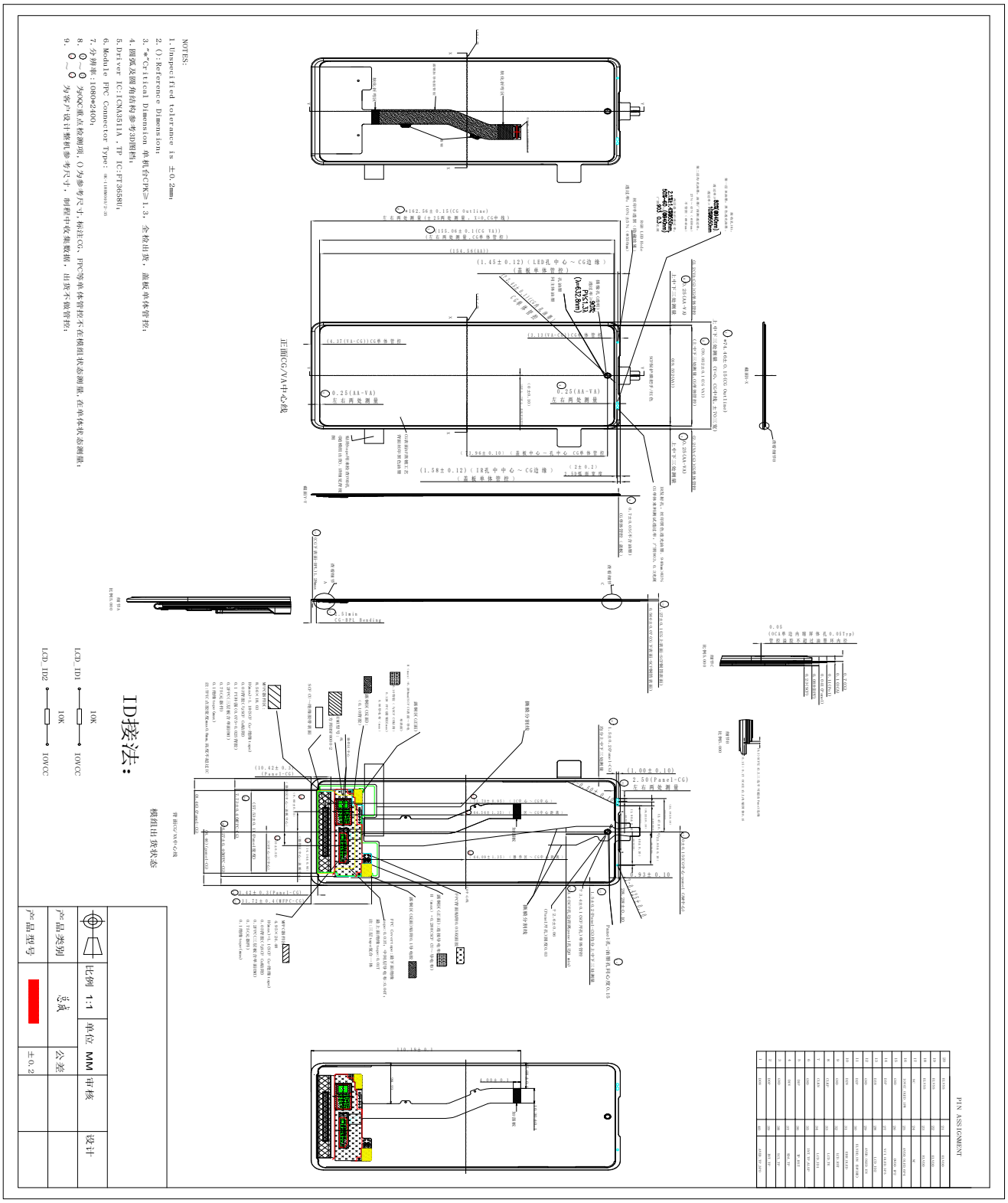
Document Revision History :

DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY
A	2024-8-26	First Release.	

1. General Specifications

No	Item	Specification	Remark
1	Screen Size	6.67 inch	
2	Display Mode	AMOLED	
3	Resolution	1080 (W) * 2400(H)	
4	Active Area	154.56(W)*69.552(H)	mm
5	Outline Dimension	162.56(W)*74.46(H)	mm
6	Color Depth	16.7M	
7	Viewing Direction	ALL	
8	Driver IC	ICNA3511A	
9	Touch IC	FT3658U	
10	Interface	MIPI	

2. Mechanical Drawing



3. Input/output Terminals

Pin No	Symbol	Description	Note
1	D0N	Negative polarity of low voltage differential data 0 signal	
2	D0P	Positive polarity of low voltage differential data 0 signal	
3	GND	Ground	
4	D1N	Negative polarity of low voltage differential data 1 signal	
5	D1P	Positive polarity of low voltage differential data 1 signal	
6	GND	Ground	
7	CLKN	Negative polarity of low voltage differential clock signal	
8	CLKP	Positive polarity of low voltage differential clock signal	
9	GND	Ground	
10	D2N	Negative polarity of low voltage differential data 2 signal	
11	D2P	Positive polarity of low voltage differential data 2 signal	
12	GND	Ground	
13	D3N	Negative polarity of low voltage differential data 3 signal	
14	D3P	Positive polarity of low voltage differential data 3 signal	
15	GND	Ground	
16	IOVCC_OLED_1P8	Power supply for display logic circuit (I/O)	
17	NC	No Connection	
18	ELVSS	Negative power supply for EL	
19	ELVSS		
20	ELVSS		
21	ELVDD	Positive power supply for EL	
22	ELVDD		
23	ELVDD		
24	NC	No Connection	
25	AVDD_OLED_6P4	Display analog circuit power	
26	DVDD_1P2	Display digital circuit signal	
27	VCI_OLED_3P3	Power supply for display analog circuit	
28	LCD_ID2	LCM ID2 Connected 10k to Iovcc	

29	**AVDD_OLED_EN**	**Enable for AVDD of DCDC Converter**	
30	**ELVDD_ON(SWIRE)**	**Enable for ELVDD&ELVSS of DCDC Converter**	
31	**ERR_OLED**	**MIPI error flag signal**	
32	**LCD_RST**	**Display reset. Active low**	
33	**LCD_TE**	**Sync Signal for preventing Tearing Effect**	
34	**LCD_ID1**	**LCM ID1 Connected 10k to Iovcc**	
35	**INT_TP_ALSP(NC)**	**No Connection**	
36	**TP_RST**	**TP reset signal. Active low**	
37	**SDA_TP**	**TP data signal**	
38	**SCL_TP**	**TP CLK signal**	
39	**INT_TP**	**TP int signal**	
40	**AVDD_TP_3P0**	**TP Analog input power**	

4. Absolute Maximum Ratings

It defines the maximum operating conditions for the DDIC device. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply Voltage for I/O	VDDI ~ VSS	– 0.3 to + 4.5	V
LDO Output	VDD ~ VSS	– 0.3 to + 1.26	V
LDO Output	VDDM ~ VSS	– 0.3 to + 1.26	V
LDO Output	VDDP ~ VSSP	– 0.3 to + 1.26	V
LDO Output	V0H ~ AVSS	– 0.3 to + AVDD	V
LDO Output	AVSS ~ V0L	+ 0.3 to – AVDD	V
LDO Output	AVSS ~ V1L	+ 0.3 to – AVDD	V
Supply Voltage for Analog	VCI ~ AVSS	– 0.3 to + 4.5	V
Supply Voltage for Analog	AVDD ~ AVSS	– 0.3 to + 9.5	V
Step-up Circuit	VOUT2 ~ AVSS	– 0.3 to + 15.0	V
LDO Output	VGH ~ AVSS	– 0.3 to + 15.0	V
Regulator Output	I_ELVDD ~ AVSS	– 0.3 to + AVDD	V
LDO Output	VREG1 ~ AVSS	– 0.3 to + AVDD	V
LDO Output	VGS ~ AVSS	– 0.3 to + AVDD	V
Step-up Circuit	AVSS ~ VOUT4	+ 0.3 to – AVDD	V
Regulator Output	AVSS ~ I_ELVSS	+ 0.3 to – AVDD	V
Regulator Output	AVSS ~ VINIT1	+ 0.3 to – AVDD	V
Step-up Circuit	AVSS ~ VGL	+ 0.3 to – 15.0	V
Restriction	VOUT2 ~ VGL	|VOUT2 – VGL| < + 20V	V
	AVSS ~ VGL	VGL < AVSS	V
	V0H - V0L	|V0H-V0L| < 9.5V	V
Supply Voltage for OTP	VPP ~ VSS	– 0.3 to + 9.5	V
MIPI Differential Input	CLKP/CLKN DATAnP/DATAnN ~ VSSM	– 0.3 to + 1.8	V
Input Voltage Range	V_{in}	– 0.3 to VDDI + 0.3	V
Output Voltage Range	V_o	– 0.3 to VDDI + 0.3	V
Operating Temperature	T_{opr}	– 40 to + 85	℃
Storage Temperature	T_{stg}	– 55 to + 125	℃

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***NOTE:**

1. Absolute maximum ratings are the limit value of operating. Beyond those ranges, the IC cannot guarantee the safety. Conditions outside the range listed in the above table may cause permanent damage to the device, may not be recovered.

2. Absolute voltages are referenced to ground.
3. DATAnP/DATAnN, n = 0, 1, 2 and 3.

***CAUTION:**

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

5 . Electrical Characteristics

DC Characteristics for Power Supply Voltage						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage for I/O	VDDI	–	1.65	1.80	1.95	V
Supply Voltage for Analog	VCI	–	2.65	3.00	3.60	V
Supply Voltage for Analog	AVDD	–	6.00	7.30	7.70	V
Supply Voltage for OTP	VPP	–	5.50	6.0	6.00	V

***NOTE:** T_A = -40 to 85℃

DC Characteristics for Generated Voltage						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
LDO Output	VDD	-	1.05	1.15	1.25	V
LDO Output	VDDM	-	1.05	1.15	1.25	V
LDO Output	VDDP	-	1.05	1.15	1.25	V
LDO Output	V0H	-	0.50	3.00	6.00	V
LDO Output	V0L	-	-6.00	-3.00	-0.50	V
LDO Output	V1L	-	-6.00	-3.00	-0.50	V
Step-up Circuit	VOUT2	-	7.00	8.00	10.00	V
Step-up Circuit	VGL	-	-3.00	-7.00	-10.00	V
LDO Output	VGH	-	3.00	7.00	9.50	V
Regulator Output	I_ELVDD	-	2.60	4.60	5.70	V
LDO Output	VREG1	Without ELVDD Compensation	2.70	7.00	7.30	V
		With ELVDD Compensation	4.80	7.00	7.30	V
LDO Output	VGS	Without ELVDD Compensation	0.20	1.50	5.30	V
		With ELVDD Compensation	0.20	1.50	4.40	V
Step-up Circuit	VOUT4	-	-2.00	-4.00	-6.50	V
Regulator Output	I_ELVSS	-	-0.50	-1.50	-5.00	V
Regulator Output	VINT0		0.50	3.00	6.00	V
			-6.00	-3.00	-0.50	V
Regulator Output	VINT1	-	-0.50	-3.00	-6.00	V

***NOTE:** T_A = -40 to 85℃

DC Characteristic for Interface Signals						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Logic High Level Input Voltage	V_{IH}	–	0.8×VDDI	–	VDDI	V
Logic Low Level Input Voltage	V_{IL}	–	VSS	–	0.2×VDDI	V
Logic High Level Output Voltage	V_{OH}	IOUT = –1mA	0.8×VDDI	–	VDDI	V
Logic Low level Output Voltage	V_{OL}	IOUT = +1mA	VSS	–	0.2×VDDI	V
Logic High Level Leakage	I_{IH}	VIN = VDDI	–	–	1.00	μA
Logic Low Level Leakage	I_{IL}	VIN = VSS	– 1.00	–	–	μA

***NOTE:** T_A = -40 to 85℃

DC Characteristic for Source Output						
Category	Symbol	Condition	MIN	TYP	MAX	Unit
Source Output Range	S<n>	–	0.20	–	7.30	V
Source Output Deviation: mean value (channel to channel)	$V_{DEV,POS}$	–	–	–	±5	mV

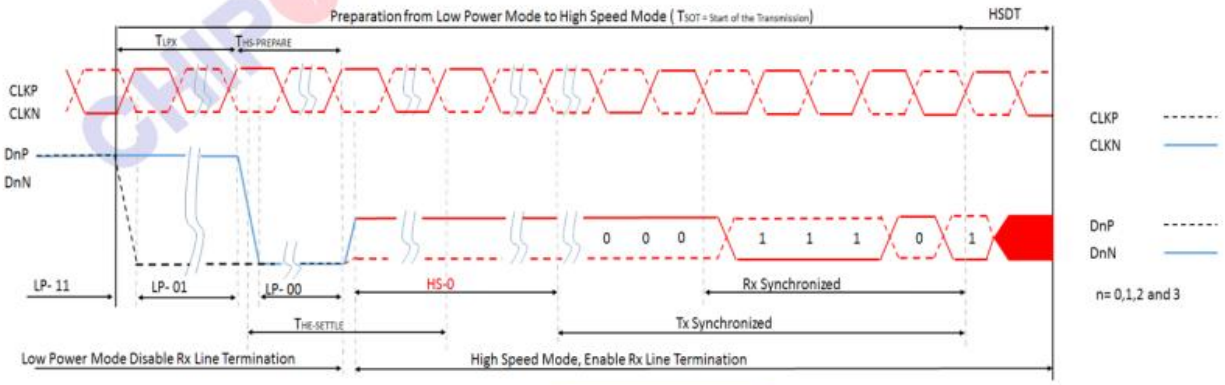
***NOTE:** T_A = -40 to 85℃

6 .AC Characteristics

6.1 MIPI Interface Characteristics

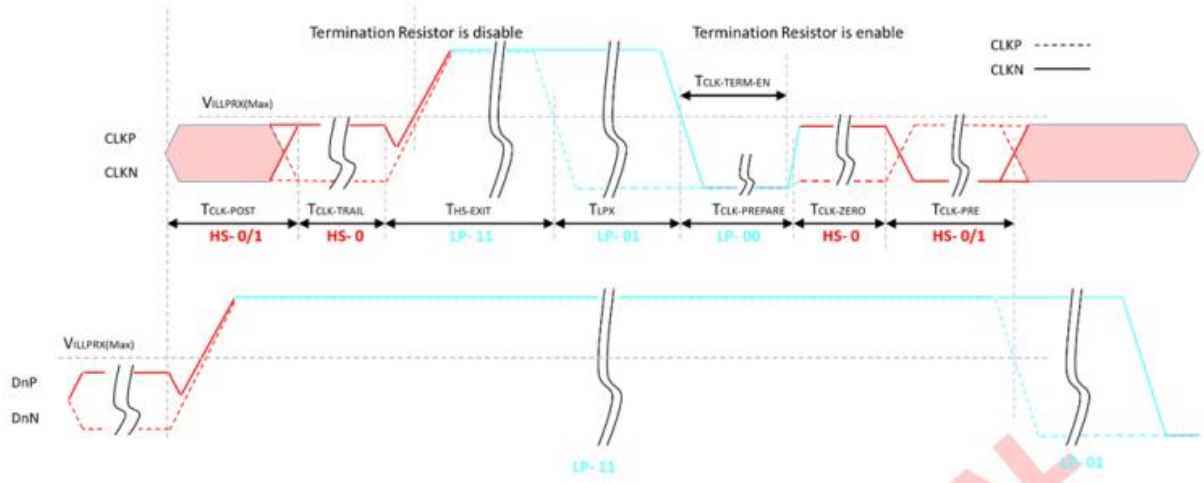
HS Data Transmission Burst

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated as below.



Entering High- Speed Data Transmission (TSOT of HSDT)

HS clock transmission



DSI Clock Burst – High-Speed Mode to /from Low-Power Mode Timing

Timing Parameter:

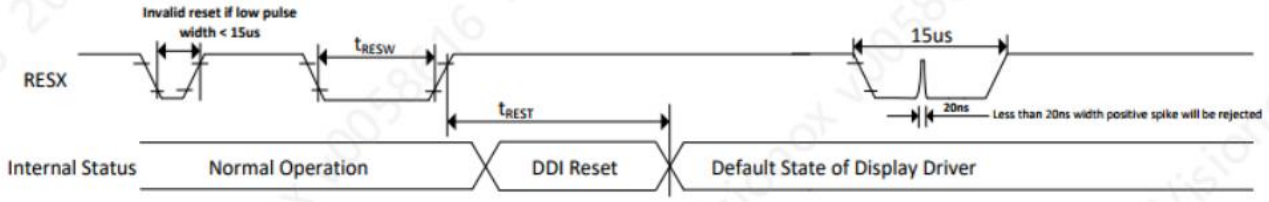
DSI Clock Burst – High-Speed Mode to /from Low-Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Note
			MIN	TYP	MAX		
CLKP/N	$T_{CLK-POST}$	Time that the AP shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CLKP/N	$T_{CLK-PREPARE}$+ $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

***Note:** DnP/N, n =0, 1, 2 and 3.

6.2 Display RESET Timing Characteristics

Reset input timing:



Reset timing @VDDI=1.65V to 3.6V, Ta=-40℃ to 85℃

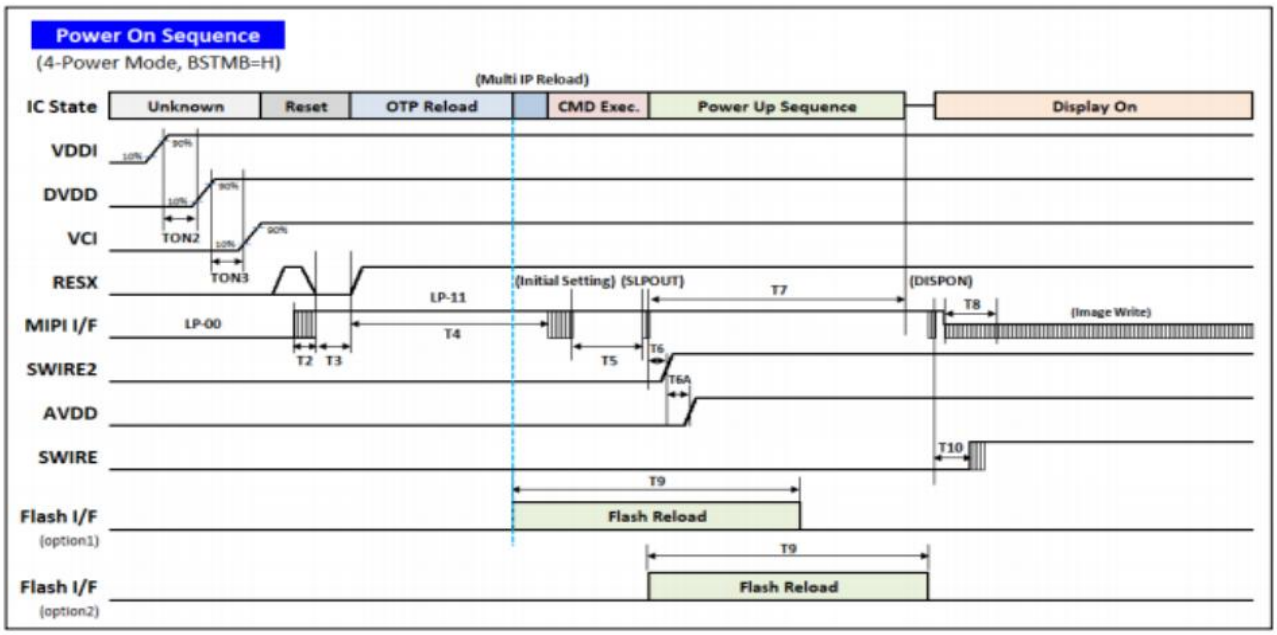
Timing Parameters

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	Reset low pulse width	15	-	-	1. Shorter than 5us, Reset rejected 2. Longer than 15μs, IC reset 3. Between 5μs and 15μs, It depends on voltage and temperature condition.	μs
t_{REST}	Reset complete time	-	-	10	When reset applied at sleep-in mode	ms
		-	-	120	When reset applied at sleep-out mode	ms

7 . Recommended Operating Sequence

7.1 Display Power on / off Sequence

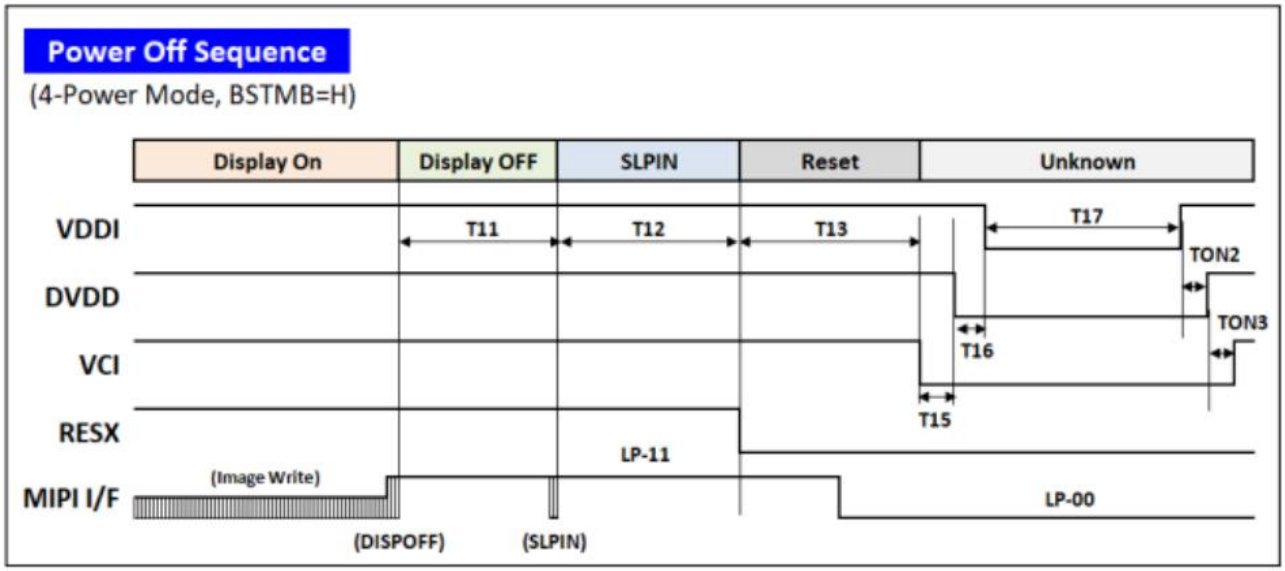
Power On Sequence



◆ **Timing Specification of Power On/Off Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
TON1	2	-	-	ms	VDDI-to-VDDI Power Ready Timing (for 3-Power Mode)
TON2	0	-	-	ms	VDDI-to-DVDD Power Ready Timing (for 4-Power Mode)
TON3	2	-	-	ms	DVDD-to-VCI Power Ready Timing (for 4-Power Mode)
T2	1	-	-	ms	MIPI stabilization time
T3	1	-	-	ms	Effective hardware reset period
T4	32	-	-	ms	Initial code input starts to RESX goes H. T4 contains OTP Reload + Multi IP Reload inside Flash IC, Note (1)
T5	0	-	-	ms	Initial code input finish to SLPOUT command input
T6	0	-	16	ms	SWIRE2 goes H after SLPOUT cmd, Note (2)
T6A	0	-	16	ms	AVDD starts after SWIRE2 goes H
T7	6	6	6	VS	Normal power-up sequence, Note (3)
T8	2	-	14	VS	Display-On Blanking region, Note (4)
T9	0	80	-	ms	16Mb Quad-SPI Flash reload time, Note (5)
T10	1	-	7	VS	SWIRE enable after receiving DISPON cmd, Note (6)
T11	1	-	14	VS	Display Off Blanking region
T12	1	-	-	VS	Power Off Blanking region
T13	2	-	-	ms	Effective hardware reset period
T14	2	-	-	ms	Power off period (for 3-Power Mode)
T15	2	-	-	ms	Power off period (for 4-Power Mode)
T16	0	-	-	ms	Power off period (for 4-Power Mode)
T17	5	-	-	ms	Power down period, Not (7)

7.2 Power Off Sequence



8. Touch Specification

8.1 General Specifications

NO	ITEM	SPEC	REMARK
1	Accuracy @D7mm Finger(mm)	Center：1.0mm Edge：1.5mm	
2	Linearity @ D7mm Finger(mm)	Center：1.0mm Edge：1.5mm	
3	Jitter @D7mm Finger(mm)	≦0.8mm	
4	Gesture Wakeup	Double tap	
5	Moisture	No line broken on diameter=10mm water puddle wet finger operation no ghost finger with water dropping	
6	Glove	2mm thickness Glove OK	
7	Touch Point	10 fingers	
8	Report Rate	240Hz@10 fingers	
9	two finger seperation	＜12mm(6mm 铜棒直径)	需要以实测为准
10	first touch latency	30ms @100Hz report rate	

8.2 Electrical Characteristics

8.2.1 Maximum Ratings

Item	Symbol	Min	Max	Unit
TP power supply input	TP_AVDD	-0.3	3.9	V
TP power supply for logic circuits	TP_DVDD	-0.3	3.9	V

8.2.2 Power supply DC characteristics

Item	Symbol	Min	TYP	Max	Unit
TP power supply input	TP_AVDD	2.7	2.8/3.0/3.3	3.4	V
TP power supply for logic circuits	TP_DVDD	1.65	1.8	1.95	V

8.3 TP FPC Pin Assignment

Pin No	Symbol	Description	Note
1	GND	Ground	
2	TP_VDD	Power Supply For TP	
3	TP_SDA	Serial data input/output pin For TP	
4	TP_SCL	Serial clock signal pin For TP	
5	TP_INT	TP interrupt request	
6	TP_RESET	Reset Signal input pin For TP	
7	GND	Ground	

8.4 Touch Design

Item		Description	Notes
Touch Design	Sensor structure	Oncell	
	Sensor pitch	Tx:4.3148 , Rx:4.186	mm
	Sensor pattern	Metal mesh	
	CH Number	16 (TX) /37 (RX)	
	Trace mode	2T1R	

9. Optical Characteristics Optical Specification

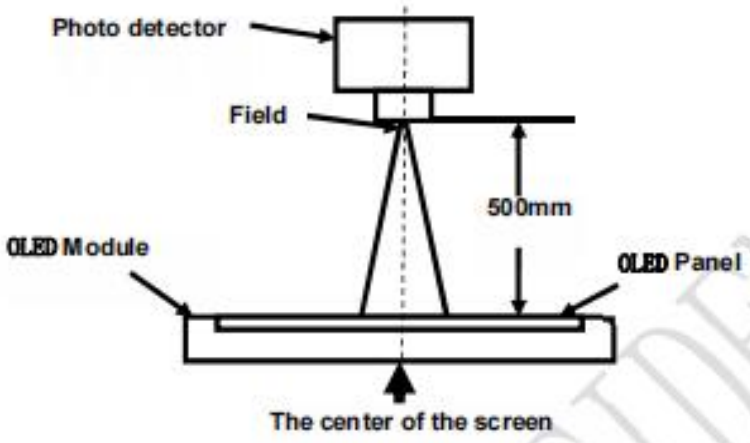
View Angles		θT	CR≧10	80	-	-	Degree	Note 2
		θB		80	-	-		
		θL		80	-	-		
		θR		80	-	-		
Contrast Ratio		CR	θ=0°	5000000	-	-	-	Note1 Note3
Response Time		T_{ON}	25℃	-	-	1	ms	Note1 Note4
		T_{OFF}						
Chromaticity	White	x	-	0.279	0.299	0.319	-	Note1 Note5 Customer can adjust white coordinate freely
		y		0.295	0.315	0.335		
	Red	x		0.65	0.68	0.71		
		y		0.29	0.32	0.35		
	Green	x		0.209	0.249	0.289		
		y		0.674	0.714	0.754		
	Blue	x		0.109	0.139	0.169		
		y		0.015	0.045	0.075		
Uniformity		U	-	80	-	-	%	Note1 Note6
Life time		L	T95, 25℃	300			hrs	
Crosstalk		C t	500/100nits			2	%	Note7
Color shift (W)		JNCD	30°/45°/60°			4/5/7	JNCD	Note1 Note2
Luminance (with Lens)		L	Normal	450	500	550	cd/m^2	Note1 Note7 TM module for reference
Luminance (with Lens)		L	HBM	900	1000	1100	cd/m^2	

Test Conditions:

1. The ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel.



Item	Photo detector
Contrast Ratio	PR730
Luminance	
Chromaticity	
Lum Uniformity	
Response Time	DMS803

Fig. 1 Optical measurement system

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the OLED by PR730.

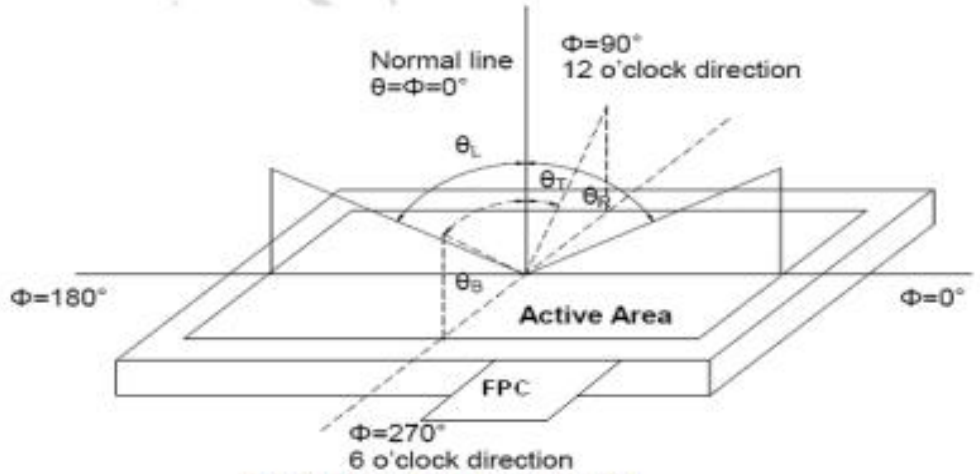


Fig. 2 Definition of viewing angle

Note 3: Definition of contrast ratio

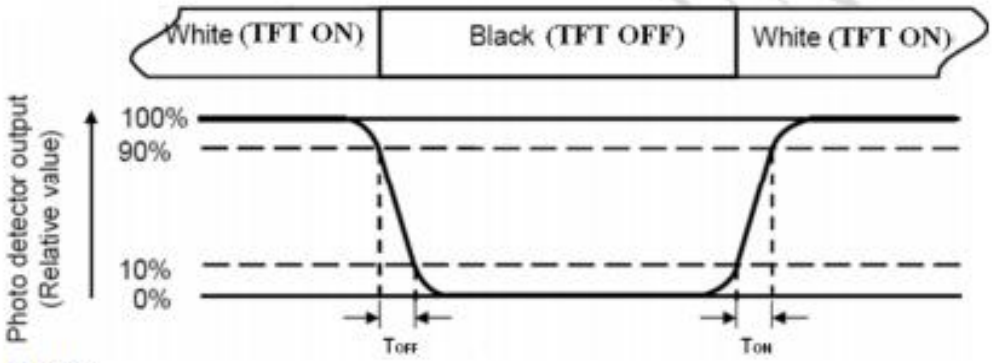
$$\text{Contrast ratio(CR)} = \frac{\text{Luminnace measured when OLED is on the "White" state}}{\text{Luminnace measured when OLED is on the "Black" state}}$$

"White state ":The state is that the OLED should be driven by Vwhite.

"Black state": The state is that the OLED should be driven by Vblack.

Note 4: Definition of Response time

The response time is defined as the OLED optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10%



to 90%.

Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of OLED.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 3). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax

L-----Active area length W---- Active area width

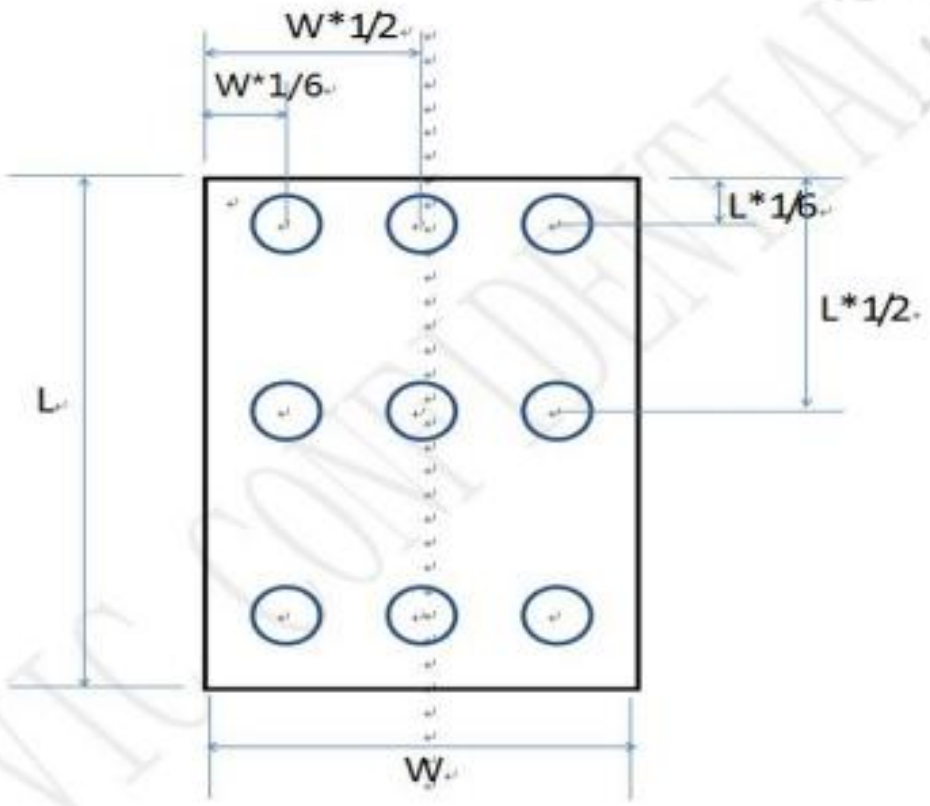


Fig. 3 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.

Lmin: The measured minimum luminance of all measurement position.

Note 7: Definition of Luminance :

Measure the luminance of white state at center point.

10. Quality Level

10.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

(1) Ambient temperature: 23± 3℃

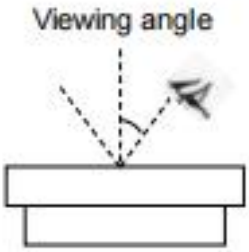
(2) Humidity: 55 ± 10%RH

(3) Ambient light intensity of visual inspection: 800 ~1300 lux

(4) Ambient light intensity of electrical inspection: <200lux

(5) Viewing Distance: 30~35cm

(6) Viewing angle: ±45°



10.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2012 Inspection level Ⅱ normal inspection single sample inspection	0.4
Minor defect	GB/T2828.1-2012 Inspection level Ⅱ normal inspection single sample inspection	0.65

Major defect:
Any defect may result in functional failure, or reduce the usability of product for its purpose. For example, no display, abnormal display, bright lines, dark lines, dimensional mismatch, etc.

Minor defect:
A defect does not reduce the usability of product for its intended purpose, such as bright and dark dot, foreign body, scratch, bubble, un-uniformity display, etc.

The criteria on major and/or minor judgment will be according with the degree of impact on the quality of product.

10.3 Appearance Inspection Item

No	Item	Level Surface	Criterion of Inspection	Defect Type
1	Dot defect(visible in appearance and invisible in light mode, AA area)	Level 0/1	1.D≤0.1mm,N ignore;	Minor
			2.0.1 mm < D≤0.2mm, DS≥10, N≤2;	
			3.0.2mm< D, NG	
2	Line defect(visible in appearance and invisible in	Level 0/1	1.W≤0.03mm, ignore	Minor
			2.0.03mm<W≤0.05mm, L≤5mm, N≤2; DS≥5	

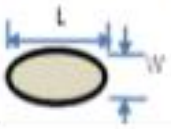
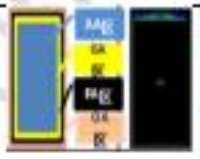
	light mode, such as fine scratch, filament, etc. AA area)		3.0.05mm<W or L>5mm, NG	
3	Crack	/	Not allowed	Major
4	Hard scratch	Level 0/1	Not allowed	Minor
5	Bubble	Level 0/1	D≤0.15mm, DS≥10mm , N≤2	Minor
6	Scratch and bubble of Cover film	Level 0/1	If no damage to the Mod , not controlled ; Damage to the Mod , controlled by point and line defect	Minor
7	Handwriting, visual mark,etc.	/	Not allowed	Minor
8	Lamination dirt	Level 0/1	According to criterion of dot and line, limit sample control if necessary	Minor
9	Cover Chromatism	Level 1	Not allowed(refer to limit sample if necessary)	Minor
10	Cover edge cutting serration	Level 1	Not allowed (refer to limit sample if necessary)	Minor
11	Cover edge paint loss	Level 1	Not allowed (refer to limit sample if necessary)	Minor
12	Flexible Cover edge breakage	Level 1	Acute defect is not allowed, quantitative criteria will be defined later	Minor
13	Flexible CG edge breakage	Level 2	Not allowed (refer to limit sample if necessary)	Major
14	Cover side damage	Level 1	Not allowed (refer to limit sample if necessary)	Minor
15	Cover ink crack	Level 1	Not allowed	Minor
16	Cover edge corrosion	Level 1	Not allowed (refer to limit sample if necessary)	Minor
17	BM/silk-screen printing ink serration	Level 0	W≤0.1mm , D≥2mm , N ignore ; 0.1< W≤0.15mm , D≥10mm , N≤2 ; Refer to limit sample if necessary	Minor

18	Indentation	Level 0/1/2	refer to limit sample		Minor
19	FPCA	Level 2	Broken line, defect	Copper foil is not allowed to have broken line and defect (width≥1/4 line width).	Minor
			Scratch	FPC can't have scratches. Hard scratch (length≥2mm) is not allowed. Circuit damaged is not allowed.	Minor
			Unfilled corner	FPC can't have unfilled corner(area≥2mmX2mm). Circuit damaged is not allowed.	Minor
			Damaged edge	FPC can't have damaged edge(length≥1mm or depth≥1mm). Circuit damaged is not allowed.	Minor
			Foreign body	Dirt or foreign body is not allowed on the FPC gold finger.	Minor
			Blister	FPC is not allowed to blister.	Minor
			Burrs	Burrs≤0.1 is acceptable. Subject to matching with actual shell material if exceeds.	Minor
			Hardcore crease	Not allowed	Major
			Breakage	The top coating of component is not allowed to be damaged in the range from the edge ≥ 0.25mm in the length direction.	Minor
			Less component	Less component is not allowed.	Minor
			Fracture	Component is not allowed to be fractured.	Minor
			Component weld wrong	Component welding reversely is not allowed.	Minor
			Golden finger	Golden finger wrinkle/dart: sharp corner wrinkle/dart are not allowed.	Minor
			Connector	Connector is not allowed to be damaged.	Minor
20	The size of BM area on both sides is different in lamination process.	Level 1	Not allowed		Minor
21	Pull glue	Level 0	The distance from PI edge to the inner edge of glue is ≤ 1.5mm.		Minor

22	Bump point	Level 0	refer to limit sample	Minor
23	Package	Level 2	Mildew, moisture, wet, dirty, deformed, damaged, mixed are not allowed. standard of Visionox label must be attached	Major
			Stacking method should be neat and order.Disorder and scatter are not allowed.	Minor
			The material code, specification model, quantity, weight, production date, production batch, and version number must be clearly identified. The repair product must have the "maintenance product" logo.	Minor

10.4 The term definition of defect

V/A: View Area , L: Length , W : width , Z : thickness , D : Diameter , DS :Distance

Name filed	PIC	Specification	Name filed	PIC	Specification
Point defects (particle/Concave point and convex point)		D=(L+W)/2	The Sawtooth definition		W: Sawtooth, the distance from the crest to the trough
Angle chipping		X Direction: parallel to FOG PAD Y direction: perpendicular to FOG PAD	Line Defect (Contains the scratch)		
Edge chipping		X direction: parallel to the edge of the screen Y direction: perpendicular to the edge of the screen Z direction: screen thickness direction			
Dark point three connection		Adjacent R, G and B pixels are not bright at the same time	Dark point two connection		Two adjacent sub-pixels are not bright at the same time
Schematic diagram of screen area		AA: Display area GA:GIF area FA: Frit area OA :edge area Include FA and GA area	Lead area		Screen GI circuit area, screen data circuit area
Bonding Area		FOG binding on LTPS base board to mark and bind PAD	LTPS PAD edge unbound zone		LTPS test PAD, cutting area, no lead area

10.5 Module Function Inspection Item

No	Item	Level Surface	Criterion of Inspection	Defect Type
1	Dot defect(visible in light mode)	Level 0	D≤0.1mm, N ignore	Minor
			0.1 mm<D≤0.2mm,DS≥10,N≤2	
			0.2mm< D, NG	
2	Bright /slight light dot	Level 0	Not allowed	Minor
3	Dark dot	Level 0	N≤2, No obvious flicker	Minor
	Pocking dot	Level 0/1	In the area of 10 mm x 10 mm, if there is a dense point of D ≤ 0.1 mm, which is judged to be pocking dot. Other point defect of D ≤ 0.1 mm , is not applicable to pocking dot under negligible condition.	
			D≤0.1mm, N≤5 , judge as other dot; N>5, Not allowed, refer to limit sample if necessary. Adjacent point is not allowed to be dense.	
	All dot	/	N≤4	
4	Line defect(visible in light mode, such as fine scratch, filament, etc.)	Level 0	W≤0.03mm, ignore	Minor
			0.03mm<W≤0.05mm, L≤5mm, N≤2 ,DS≥5	
			0.05mm<W ,L>5mm, NG	
5	TP function NG		Not allowed	Major
6	Bubble	Level 0/1	D≤0.15mm, DS≥10mm,N≤2	Minor
7	No display/ abnormal display/ can't switch	Level 0	Not allowed	Major
8	Bright line/ multiple bright line, dark line, half line	Level 0	Not allowed	Major
9	Mura(include yellowing)	Level 0	Class A customer standard (refer to limit sample control if there is any objection).	Minor
10	ELA Mura	Level 0	refer to limit sample	Minor
11	Etched lines	Level 0	Not allowed in light mode, check sample if necessary.	Minor
12	Other defects	Level 0/1/2	Subject to the sealed sample, develop limit samples if necessary.	/
13	Color deviation	Level 0	Not allowed (refer to limit sample if necessary)	Minor
14	Leakage around	Level 0	Not allowed	Minor

Note: If some product specifications are not clearly defined, they will be not allowed in control.

Level surface instruction:

Level 0: Important areas such as information or taking photo on the phone. For example, AA display area, camera hole area, ICON silk screen area, IR hole area.

Level 1: The main surface exposed can be seen directly during normal use, such as the front side except level 0. For example, non-display area outside AA area, CG ink area.

Level 2: The reverse side of screen except camera hole, ICON, and IR hole area, such as FPC.

11. Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+70℃, 240hrs	Note1
2	Low Temperature Operation	Ta=-20℃,240hrs	
3	High Temperature Storage	Ta=+80℃, 240hrs	
4	Low Temperature Storage	Ta=-40℃, 240hrs	
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH 240 hours	Note2
6	Thermal Shock (Non-operation)	-40℃ 30 min~+80℃ 30 min, Change time:3min, 100Cycles	Start with cold temperature, End with high temperature,
7	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)(Package condition)	
8	Package Drop Test	Height:80 cm,(When Package weight 10≤M<20 Kg) 1 corner, 3 edges, 6 surfaces	

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

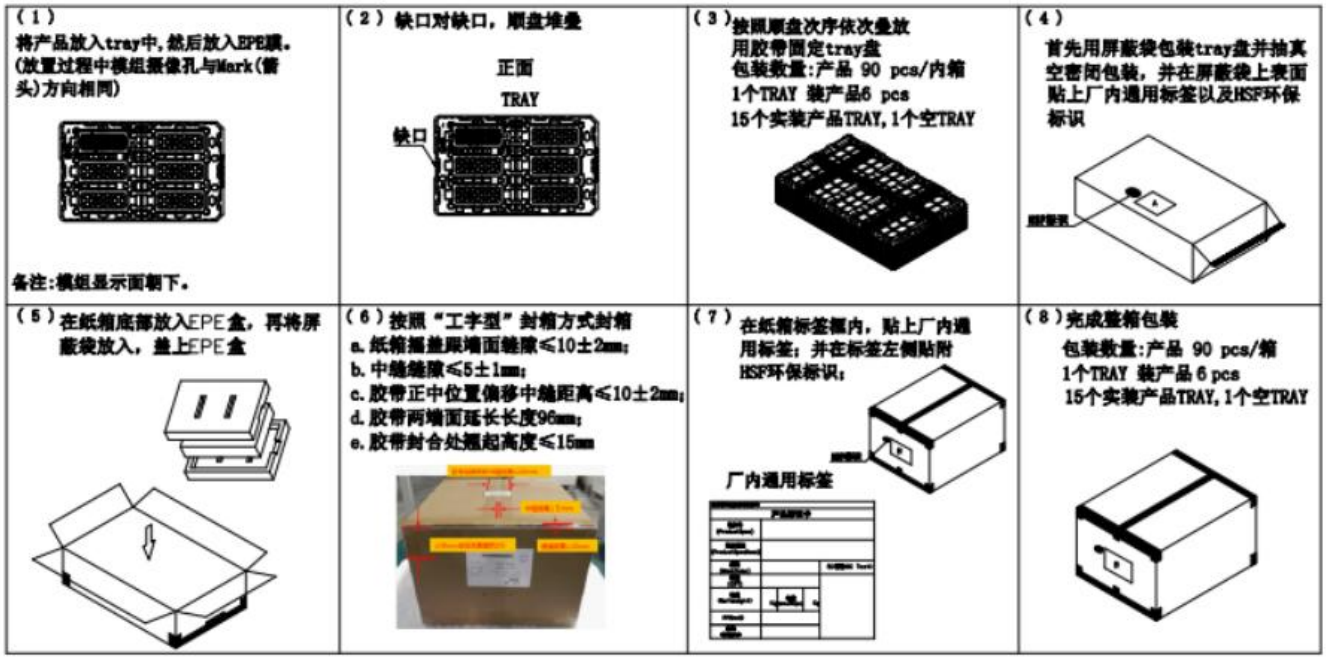
Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

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Packing Drawing

TBD



Packing Condition	Contents
Packing Type	TRAY + Carton packing type
TRAY material model	tray (10^4~$10^9\Omega$)
Tray packing type	See the picture 1
Number of panels per tray	6 pieces
Number of Tray per carton	16units ((15 units + 1 empty)PET tray)
Number of panels per carton	90 pieces

12. Precautions for Use of AMOLED Modules

12.1 Handling Precautions:

12.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.

12.1.2 Do not press down the screen or the adjoining areas too hard because the color tone may be shifted.

12.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.

12.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.

12.1.5 Solvents may damage the polarizer. Do not use water, ketone or aromatic solvents except ethyl alcohol.
Do not attempt to disassemble the AMOLED Module.

12.1.6 If the logic circuit power is off, do not apply the input signals.

12.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.

12.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.

12.1.9 Tools required for assembly, such as soldering irons, must be properly ground.

12.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.

12.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

12.2 Storage Precautions:

12.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.

12.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is: Temperature: 0℃~40℃ Relatively humidity: ≤80%

12.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

12.3 Transportation Precautions:

12.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.